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Wen, D.S.; Hsu, C.C.-H.; Taur, Y.; Zicherman, D.S.; Wordeman, M.R.; Ning, T.
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Chen, M.-L.; Hillenius, S.J.; Juengling, W.; Yang, T.S.; Kornblit, A.; Lindenberge
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3 A self-aligned LDD/channel implanted ITLDD process with selectively deposited poly gates for CMOS VLSI

Pfiester, J.R.; Baker, F.K.; Sivan, R.D.; Crain, N.; Lin, H.-H.; Liaw, M.; Seelbach
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